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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/530,465	07/13/2000	YAU WEI LUCAS HUI	851663.408	7060

7590 04/16/2004

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EXAMINER	
LAM, DANIEL K	
ART UNIT	**PAPER NUMBER**
2667	6

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/530,465	HUI ET AL.	
	Examiner	Art Unit	
	Daniel K Lam	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 July 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The following informalities are objected to:

   - In claims 1 and 13, line 15, 'these" is misspelled. It should be "them" instead.
   - In claims 6 and 18, line 3, "relaced" is misspelled. It should be "replaced" instead.

   Appropriate corrections are required.

Claim Rejections - 35 USC § 112

2. There are insufficient antecedent basis in the following claim limitations:

   - Claims 1 and 24 recite the limitations of "the input data" in line 4, "said words" in line 10, and "said separate receiving" in line 14.
   - Claims 2, 11, 12, 15, 26, 28, and 29 recite the limitations of "the input data".
   - Claim 5, recites the limitation of " said packetized data source" in line 5.
   - Claim 6 recites the limitations of "said input data" in line 2, "said words" in line 3, and "to the data" in line 4.
   - Claim 13, recites the limitations of "the input data" in line 3, "the size" in lines 5 and 8, "the input outputted" in line 6, "the word formatter" in line 10, "said word formatter" in lines 12 and 14.
   - Claim 14, recites the limitation of "said input data" in line 3.
   - Claim 16, recites the limitations of "said level-filled signal" in line 2, and "the data packet" in line 4.

- Claim 17, recites the limitations of "said data input interface" in lines 2 and 3, "said packetized data source" and "the data transmission rate" in line 5.
- Claim 18, recites the limitations of "said input data" and "a said packet" in line 2, "the data processor" in line 4.
- Claim 19, recites the limitation of "the data processor" in line 5.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. **Claims 1, 6, 10-13, 18, and 20-25 are** rejected under 35 U.S.C. 102(e) as being anticipated by U. S. Pat. No. 5,963,596 issued to Benbassat et al (hereinafter Benbassat).

Regarding **claims 1, 13, 24, and 25,** Benbassat discloses a decoder apparatus and its method of operation comprising:

- System decoder block 20 receives data from host interface block 18 and stores them into FIFO 38 (see fig. 2 and col. 8, lines 52-53) and, then, into input buffer 24 (see fig. 1 and col. 4, lines 12-14). The data are processed by the audio decode block 28 (An input memory for receiving and storing the input data packet; claims 1 and 24. Receiving and storing the input data in an input memory, and outputting the stored input data to data processing means; claims 13 and 25).
- A control logic block 46 has a state machine controlling the overall execution of the system decoder block 20 (see fig. 2, and col. 9, lines 28-30). It works together with a hardware filter arithmetic unit block 32 and a PCM output block 36 (see fig. 1 and col. 5, lines 17-22) forming the data processing engine for complete decoding for the audio information (Data processing means for receiving, identifying, determining payload size of the data packet, separately receiving and effecting data processing using received data words; claims 1 and 24. By use of the data processing means detecting, identifying, determining, and generating a signal for payload size; claims 13 and 25. Effecting data processing on the data packet represented by the data words; claim 13).
- The audio decoder block 28 breaks the received data into coded sample, and then, into framed PCM data (A word formatter for receiving, gathering and aligning of the units to form data words; claims 1 and 24. By use of said word formatter, gathering

and aligning said payload units; claims 13 and 25). See fig. 1, and col. 4, and lines 47-56.

- During the execution of the control logic block 46, at step 70, the packet data count is extracted from the packet header and loaded into the packet byte counter 72. When the packet byte counter becomes zero, the control logic 46 returns to step 60 to search for a start code (A payload counter for controlling the input memory with the payload size signal; claims 1 and 24. Controlling the input memory with the payload size signal; claims 13 and 25). See fig. 2, and col. 10, lines 24-26 and line 61-63.
- After the data is being decoded and filtered, they are stored in the PCM buffer 34 and, then, transferred to the D/A 16 by the PCM output block 36 (An input buffer for receiving and storing the data words from the word formatter, and transferring the data words to the data processing means; claims 1 and 24. Outputting said data words to an input buffer and transferring said data words to the data processing means; claims 13 and 25). See fig. 1, and col. 5, and lines 20-22.

Regarding **claims 6 and 18**, in addition to disclose the limitations in claims 1 and 13 discussed earlier, Benbassat further discloses that the audio decoder system 14 retrieves the MPEG audio data from the FIFO and input buffer. Then the system decoder block 20, audio decoder block 28, and hardware filter arithmetic unit block 32 process the retrieved data. The data are then stored in the PCM buffer 34 to be transmitted by the PCM output block 36 to the D/A 16. During the processing, the format of the data and the size of the payload are extracted (The input memory is controlled whereby said input data and the data processing means repetitively and alternating executing a step comprising

said receiving the data from the input memory and detecting, identifying and determining payload size of the data packet and generating said payload size signal, and comprising separating receiving and effecting data processing of the payload). See fig. 1, and col. 3, lines 10-18.

Regarding **claims 10 and 21**, in addition to disclose the limitations in claims 1 and 13 discussed earlier, Benbassat further discloses that the synchronization is continuous updated (see col. 6, lines 52-54) by looking for the synchronization word (see col. 6, lines 61-64). After that the control logic 46 detects the beginning of the packet at step 60 and once it is detected, begins looking for the packet header that contains the packet ID of the desired audio stream (Detecting and identifying the data packet by detection of a sync-word, followed by verification of the packet ID; claims 10 and 21). See fig. 2, and col. 10, lines 11-12.

Regarding **claims 11 and 22**, in addition to disclose the limitations in claims 1 and 13 discussed earlier, Benbassat further discloses that the system timing reference is retrieved from the packet header at step 62 (Extract timing information from the input data; claims 11 and 22). See fig. 2, and col. 10, lines 27-29.

Regarding **claims 12 and 23**, in addition to disclose the limitations in claims 1 and 13 discussed earlier, Benbassat further discloses that the side information is being extracted from the packet header (Extracting side information from the input data; claims 12 and 23). See fig. 19, and col. 36, lines 45-47.

Regarding **claim 20**, in addition to disclose the limitations in claim 13 discussed earlier, Benbassat discloses using a FIFO 38 as part of the input memory (input memory is a first in first out memory). See fig. 2 and col. 8, lines 52-53)

5. **Claims 26-29 are** rejected under 35 U.S.C. 102(e) as being anticipated by U. S. Pat. No. 5,893,066 issued to Hong.

Regarding **claims 26 and 28,** Hong discloses a MPEG audio apparatus for depacketizing and aligning packetized input data comprising multimedia multiprocessor system 100 (see fig. 2) including a host processor 100 and a multimedia signal processor 104. The multimedia signal processor interfaces to various functional blocks, such as audio and video CODEC 108, for detecting data packets and processing data payload (data processing means configured to detect a payload of a data packet and to process the payload; claims 26 and 28). See col. 2, line 66 to col. 3, line 10.

Regarding **claims 27 and 29,** in addition to disclose the limitations in claims 26 and 28 discussed earlier, Hong further discloses that the scalar processor 204 (see fig. 3) within the multimedia signal processor 104 repetitively and alternating performs various functions, such as bit manipulation on the audio data and extraction of header information from the payload (data processing means repetitively and alternatingly executes functions of detecting and processing payloads; claims 27 and 29). See col. 4, lines 3-12.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 2-5, 9, and 14-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Pat. No. 5,963,596 issued to Benbassat et al (hereinafter Benbassat) in view of U. S. Pat. No. 5,410,355 issued to Kolczynski.

Regarding **claims 2 and 14**, although Benbassat discloses the limitations in claims 1 and 13 discussed earlier, he does not disclose the input interface configured to perform handshaking with a packetized data source (claim 2) and the input data is transferred to the input memory via a data input interface that performs hand shaking (claim 14). Kolczynski, on the other hand, discloses a priority analysis FIFO buffer 22 having an interface that handshakes, using a transport ready signal, with the MPEG-like processor 14 data source. See fig. 1, and col. 7, lines 51-57.

Therefore, it would have been obvious to those having ordinary skill in the art, at the time of invention, to build a packet decoder comprising an input memory, data processing means, a word formatter, a payload counter, and an input buffer, with an interface at the input memory so that it can handshake with the data source using a signal, such as, the transport ready signal, for a key motivation. Since the data source, either audio or video, may generate a large amount of data in a short period of time, handshaking signal provides a safety mechanism to prevent data loss as taught by Kolczynski. See col. 7, lines 57-59.

Regarding **claims 3 and 15**, in addition to disclose the limitations in claim 1 and 13 discussed earlier, Kolczynski further discloses generating the transport ready handshaking signal either when the buffer 22 is full or almost full. Furthermore the control unit 24 detects read enable signal from the buffer 22 (The input memory has a fullness level detector and the data processing means is responsive to generation of the level-filled signal; claim 3. Generating a level-filled signal when the input memory is filled to a predetermined level and causing said data processing means to effect processing; claim 15). See fig. 1, and col. 3, lines 16-19.

Regarding **claims 4 and 16**, in addition to disclose the limitations in claims 3 and 13 discussed earlier, Benbassat further discloses the BALF_LIM register is used by the microprocessor host 12 to set the almost full limit for the input buffer 24 (see col. 7, lines 14-16). Furthermore, Bit 4 of the interrupt register is set when the input buffer is over the almost full limit (see col. 8, lines 29-31) (An interrupt controller for receiving said level-filled signal, generating an interrupt signal, and said data processing means arranged for receipt of said interrupt signal; claim 4. Generating an interrupt signal from said level-filled signal, directing said interrupt signal to said data processing means; claim 16).

Regarding **claims 5 and 17**, in addition to disclose the limitations in claims 4 and 15 discussed earlier, Kolczynski discloses a priority analysis FIFO buffer 22 having an interface that handshakes, using a transport ready signal, with the MPEG-like processor 14 as data source (The input memory has a further fullness level detector to said data input interface indicating of a need to modify the data

transmission rate from the packetized data source; claim 5. Generating and directing a further level-filled signal to said packetized data source, indicative of a need to modify the data transmission rate; claim 17). Also see fig. 1, and col. 7, lines 51-57.

Regarding **claims 9**, in addition to disclose the limitations in claim 5 discussed earlier, Kolczynski discloses using a priority analysis FIFO buffer 22 as input memory (input memory is a first in first out memory). See fig. 1.

8. **Claims 7, 8, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over U. S. Pat. No. 5,963,596 issued to Benbassat et al (hereinafter Benbassat) in view of U. S. Pat. No. 5,893,066 issued to Hong.

Regarding **claims** 7, although Benbassat discloses the limitations in claims 1 discussed earlier, he does not disclose the data processing means includes a digital signal processor, data/program memory, DMA controller and input buffer, each in data communication via a bus. Hong, on the other hand, discloses an apparatus for MPEG audio decoding (see figure 3) comprising:

- A Multimedia Signal Processor 104 (data processing means) comprising a DSP core 202 (a digital signal processor) that includes a scalar processor 204 and a vector processor 206. See col. 3, lines 17-19.
- Data cache 214 and instruction cache 216 (data/program memory). See col. 11, lines 17-18.
- DMA controller 224 and memory within the customer ASIC 226 (DMA controller and input memory).

- The DSP, data and instruction cache, DMA controller, and input memory are connected via FBUS 210 (each in data communication via a bus). See col. 11, lines 39-42.

Therefore, it would have been obvious to those having ordinary skill in the art, at the time of invention, to build a packet decoder comprising an input memory, a word formatter, a payload counter, an input buffer, and data processing means which includes digital signal processing capabilities for a key motivation. By having digital signal processing capabilities built into the decoder, scalar and vector operations that are essential for processing MPEG audio data packets can be separated and performed in parallel. As a result, the performance of the decoding process will be improved as taught by Hong. See col. 1, and lines 60-64.

Regarding **claims 8 and 19**, in addition to disclose the limitations in claims 7 and 18 discussed earlier, Hong discloses the DMA controller 224 and the customer ASIC logic block 226 which furnishes control logic for implementing custom functionality, as desired, including interfaces to various analog CODECs and customer-specific I/O devices. The DMA controller moves digital data from the CODEC's or customer-specific I/O devices to the SDRAM 230 that is local to the multimedia signal processor (The word formatter generates a DMA request for transferring data word to the digital signal processor from the word formatter to the input buffer for subsequent processing; claim 8. Generating a DMA request signal when a said data word is formed, and applying the DMA request signal to a digital signal processor to enable a DMA controller to move that

data word from the word formatter to an input buffer; claim 19). See fig. 2, and col. 11, lines 45-49.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel K. Lam whose telephone number is (703) 305-8605. The examiner can normally be reached on Monday-Friday from 8:30 AM to 4:30 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (703) 305-4378. The fax phone number for this Group is (703) 872-9314.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-4700.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status Information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DKL dkl
April 9, 2004

Chau T. Nguyen

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